What is claimed is:

- 1 1. An integrated circuit comprising:
- 2 a peripheral interface to receive an interrupt request;
- a memory interface to communicate with a memory device;
- 4 a processor interface to communicate with a processor; and
- 5 a logic circuit connected to the peripheral interface to acquire the
- 6 interrupt information associated with the interrupt request, wherein the logic circuit
- 7 is also connected to the processor interface and the memory interface to pass the
- 8 interrupt information to the memory device without passing the interrupt
- 9 information to the processor interface.
- 1 2. The integrated circuit of claim 1 further includes a memory unit to store the
- 2 interrupt information before the interrupt information is passed to the memory
- 3 interface.
- 1 3. The integrated circuit of claim 1 further comprising a configuration circuit to
- 2 store configuration address indicating a location in the memory device to store the
- 3 interrupt information.
- 1 4. The integrated circuit of claim 3, wherein the configuration circuit includes a
- 2 read only memory device to store the configuration address.
- 1 5. The integrated circuit of claim 1 further comprising a graphics interface to
- 2 communicate with a graphics card.
- 1 6. A system comprising:
- a processor;
- a memory device; and

- 4 a chipset connected to the processor and the memory device, wherein the
- 5 chipset is configured to receive interrupt information and to pass the interrupt
- 6 information to the memory device without notifying the processor the presence of
- 7 the interrupt information.
- 1 7. The system of claim 6, wherein the chipset includes a graphic and memory
- 2 control hub to process graphic and memory information and to provide access
- 3 between the processor and the memory device.
- 1 8. The system of claim 7, wherein the chipset further includes an input output
- 2 control hub connected to the graphic and memory control hub to process input
- 3 output information between the chipset and external devices.
- 1 9. The system of claim 8, wherein the chipset further includes an interrupt
- 2 controller to receive the interrupt information.
- 1 10. The system of claim 6, wherein the processor is configured to poll the
- 2 memory device to check for the interrupt information at a time independent from a
- 3 time the interrupt information is received by the chipset.
- 1 11. The system of claim 6 further comprising a second processor connected to
- 2 the chipset.
- 1 12. The system of claim 11, wherein the second processor is configured to poll
- 2 the memory device to check for the interrupt information at a time independent from
- a time the interrupt information is received by the chipset.

- 1 13. A method comprising:
- 2 receiving an interrupt request at an interrupt controller;
- acquiring, at the interrupt controller, interrupt information corresponding to
- 4 the interrupt request; and
- 5 passing the interrupt information from the interrupt controller to a memory
- 6 device without passing the interrupt information to a processor.
- 1 14. The method of claim 13 further comprising:
- 2 polling the memory device to check for the interrupt information.
- 1 15. The method of claim 14, wherein polling is performed by the processor at a
- 2 time independent from a time the interrupt request is received by the interrupt
- 3 controller.
- 1 16. The method of claim 14 further comprising:
- 2 performing an interrupt function based on the interrupt information.
- 1 17. The method of claim 14, wherein polling is performed by a second processor
- 2 a time independent from a time the interrupt request is received by the interrupt
- 3 controller.
- 1 18. The method of claim 13, wherein the memory device and the interrupt
- 2 controller are located in separate chips.
- 1 19. The method of claim 13, wherein passing the interrupt information from the
- 2 interrupt controller to the memory device includes writing the interrupt information
- 3 to the memory device at a memory location according to configuration information.
- 1 20. The method of claim 19, wherein the configuration information is stored in
- 2 the interrupt controller.

- 1 21. A method comprising:
- 2 receiving an interrupt request at a chipset, the chipset connecting to a
- 3 processor;
- 4 acquiring, at the chipset, interrupt information corresponding to the interrupt
- 5 request;
- 6 storing the interrupt information at a memory location without notifying the
- 7 processor the interrupt request; and
- 8 polling the memory device to check for the interrupt information, wherein
- 9 polling is performed at a time independent from a time the interrupt request is
- 10 received at the chipset.
- 1 22. The method of claim 21, wherein polling is performed by the processor.
- 1 23. The method of claim 21, wherein polling is performed by a second processor
- 2 connected to the chipset.
- 1 24. The method of claim 21 further comprising:
- 2 performing an interrupt function based on the interrupt information stored in
- 3 the memory location.
- 1 25. The method of claim 21, wherein storing the interrupt information at the
- 2 memory location includes storing the interrupt information in a memory device
- 3 separate from the processor and the chipset.
- 1 26. The method of claim 25, wherein storing the interrupt information at the
- 2 memory location includes storing the interrupt information at the memory location
- according to a configuration information.
- 1 27. The method of claim 26, wherein the configuration information is stored in
- 2 the chipset.